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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/782,509	02/12/2001	Woobin Lee	1552-7-10	7513

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EXAMINER	
DANG, DUY M	

ART UNIT	PAPER NUMBER
2621	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/782,509	LEE, WOOBIN	
	Examiner	Art Unit	
	Duy M. Dang	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2005 and 18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31 and 33-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-8,15-24,34-36 and 43-52* is/are allowed.

6)☒ Claim(s) *9-14,25-31,33,37-42 and 53-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/12/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/8/05 has been entered.

2. An advisory office action was inadvertently mailed 4/22/05 so please disregard it.

3. Applicant's arguments filed 3/8/05 have been fully considered but they are not persuasive.

In response to applicant's remarks with regard to claim 9 that Masaki does not teach storing a set of resulting values in more than one memory row, the examiner disagree. In this case, Masaki teaches these features as shown in figure 7, for example. The output of 1-D IDCT, block 1 and block 2 are written into buffers 1-2 respectively. The two rows in buffers 1-2 for storing these output from 1-D IDCT refer to claimed features.

In response to applicant's remarks with regard to claim 25, that Masaki does not teach claimed invention, the examiner disagrees. In this case, the transposition memory shown in figure 7 refers to claimed register. The buffers 1 and 2 of figure 7 in Masaki refers to claimed first continuous section of register and second continuous section of register respectively. The odd block (i.e., block1, block3,...) and even block (i.e., block0, block2,...) respective stored in buffer 1 and buffer refer to claimed every other position.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 8-14, 25-33, 37-42, and 53-59 are rejected under 35 U.S.C. 102(b) as being anticipated by Masaki et al. ("VLSI Implement of Inverse Discrete Cosine Transformer and Motion Compensator for MPEG2 HDTV Video Decoding" IEEE Transactions on Circuits and Systems for Video Technology, Vol. 5, No. 5, October 1995, pages 387-395. Art of record filed 3/4/02, paper #5).

The advanced statements in paragraph 3 above are incorporated herein.

Regarding claim 1, Masaki teaches an image decoder (i.e., decoder mentioned in abstract and shown in figure 1) comprising: a memory (see "frame memory", "buffer", and "register" shown in figure 1; and the transposition memory shown in figure 7) ; and a processor coupled to the memory and operable to (see "DSP" shown in figure 1 and mentioned in page 387, right column, last 7 lines),

store a column of intermediate values in the memory as a row of intermediate values (see "Transposition Memory" shown in figure 7 and the text portion mentioned under the "Transposition Memory" section on page 391, right column. Note that figure 6 illustrates a block of intermediate data to be stored in the transposition memory. As to figure 7, the buffer 1 stores rows of intermediate values and buffer 2 stores columns of intermediate values)

combine the intermediate values within the stored row to generate a column of resulting values (see buffers 1 shown in figure 7. Note that buffer 1 stores rows of intermediate values and the resultant of these rows of intermediate values stored in buffer 1 constitutes a column of resulting value), and

store the resulting values in the memory as a row of resulting values (see buffer 2 shown in figure 7 comprising 3 rows each comprises a block).

Regarding claim 2, Masaki further teaches Masaki values (see the "xe" ("e" refers to even) and "xo" ("o" refers to odd) shown in the equation mentioned on page 389 left column. This interpretation is consistent with applicant's disclosed on the specification page 12 lines 3-15).

The advanced statement as applied to claim 1 above are incorporated herein. Regarding claim 3, Masaki further teaches wherein the memory comprises first and second rows of storage locations (see transposition memory shown in figure 7).

Regarding claim 4, Masaki further teaches generating the column of intermediate values (see figure 6 and text portioned mentioned under the "Transposition Memory" section on page 391 right column).

Regarding claim 8, Masaki further teaches inversed transforms (see "IDCT" shown in figure 7).

The advanced statement as applied to claim 1 above are incorporated herein. Regarding claim 9, an image decoder (i.e., decoder mentioned in abstract and shown in figure 1) comprising: a first memory register (see "frame memory", "buffer", and "register" shown in figure 1; and the "transposition memory" shown in figure 7) and a processor coupled to the register and operable (see "DSP" shown in figure 1 and mentioned in page 387, right column, last 7 lines) to combine a first column of first intermediate values with a second column of second intermediate values to generate a set of resulting values and store the set of resulting values in the first memory register (see buffer 2 shown in figure 7. Note this buffer 2 comprises

a combination of first column of first intermediate values (i.e., block 0) with a second column of second intermediate values (i.e., block 2)).

Regarding claim 10, Masaki further teaches Masaki values (see the "xe" ("e" refers to even) and "xo" ("o" refers to odd) shown in the equation mentioned on page 389 left column. This interpretation is consistent with applicant's disclosed on the specification page 12 lines 3-15).Regarding claim 11, Masaki further teaches a second memory register (see buffer 2 of Transposition Memory shown in figure 7), and store the first and second intermediate values of the first and second column in the second memory register (see buffer 2 shown in figure 7 comprising "block0" and "block2").

Regarding claim 12, Masaki further teaches adding the first intermediate values to the second intermediate values (see the adder included in the IDCT shown in figure 5 and text portion mentioned in second paragraph on page 391 left column).

Regarding claim 13, Masaki further teaches subtracting the first intermediate values to the second intermediate values (see the subtracter included in the IDCT shown in figure 5 and text portion mentioned in second paragraph on page 391 left column).

Regarding claim 14, Masaki further teaches generating first column of first intermediate values and second column of second intermediate values (see figure 6 and text portion mentioned under "Transposition Memory" section on page 391 right column).

The advanced statement as applied to claim 1 above are incorporated herein. Regarding claim 25, an image decoder (i.e., decoder mentioned in abstract and shown in figure 1) comprising a processor operable (see "DSP" shown in figure 1 and mentioned in page 387, right column, last 7 lines) to:

receive pixel values that each occupy a respective position within an original row of pixel values (see "output" shown in figure 7. The positions between the "block" and "row" shown in this figure 7 refers to the so called "respective position");

store the pixel values that respectively occupy every other position of the row in a first continuous section of a register (see figure 7. Note that the "block 1" and "block 3" in buffer 1 refers to the so called "every other position"), and

store the pixel values that respectively occupy remaining positions of the row in a second continuous section of the register (see figure 7. Note buffer 2).

Regarding claim 26, Masaki further teaches even positions within the row (see figure 6a: even positions "26" (coordinated at x=2, y=2 with regard to the origin at "29" (bottom left corner of the 8x8 block)) and "28" (coordinated at x=4, y=2) within the 2nd row (row of "25, 26, 27, 28, 28, 27, 26,25")) and odd position within the row (see figure 6a: odd positions of "21" (Likewise, coordinated at x=1, y=3) and "23" (Likewise, coordinated at x=3, y=3) within a 3rd row (row of "21, 22, 23, 24, 24, 23, 22, 21")).

Regarding claim 27, Masaki further teaches the pixel values each comprises a respective encoded pixel value (see figure 6 and text portion mentioned under "Transposition Memory" section on page 391 right column. Note the pixel values stored in the transposition memory (transposed data) refer to encoded pixel values order for the IDCT to inverses its original value).

Regarding claim 28, Masaki further teaches DCT coefficient (this features is inherently included in the "encoding/decoding" mentioned on page 387, right column, lines 1-3).

Regarding claim 29, Masaki further teaches receiving a block of pixel values (see figure 6 and text portion mentioned under "Transposition Memory" section on page 391 right column.

Note that this data block is written to transposition memory and received by IDCT according to figure 7).

Regarding claim 30, it is noted that this claim recites similar features called for in claim 1 lines 4-8. Thus, claim 30 is also rejected for the same reason as set forth in claim 1 above.

Regarding claim 31, Masaki further teaches Masaki values (see the "xe" ("e" refers to even) and "xo" ("o" refers to odd) shown in the equation mentioned on page 389 left column. This interpretation is consistent with applicant's disclosed on the specification page 12 lines 3-15).

Regarding claim 32, see claim 3 rejection section above.

Regarding claim 37, it is noted that this claim recites similar features called for in claim 9 lines 4-7. Thus, claim 37 is also rejected for the same reason as set forth in claim 9 above.

Regarding claim 38, Masaki further teaches Masaki values (see the "xe" ("e" refers to even) and "xo" ("o" refers to odd) shown in the equation mentioned on page 389 left column. This interpretation is consistent with applicant's disclosed on the specification page 12 lines 3-15).

Regarding claim 39, Masaki further teaches a second memory register for storing first and second intermediate values of the first and second columns (see buffer 2 of transposition memory shown in figure 7).

Regarding claim 40, Masaki further teaches adding the first intermediate values to the second intermediate values (see the adder included in the IDCT shown in figure 5 and text portion mentioned in second paragraph on page 391 left column).

Regarding claim 41, Masaki further teaches subtracting the first intermediate values to the second intermediate values (see the subtracter included in the IDCT shown in figure 5 and text portion mentioned in second paragraph on page 391 left column).

Regarding claim 42, Masaki further teaches generating first column of first intermediate values and second column of second intermediate values (see figure 6 and text portion mentioned under "Transposition Memory" section on page 391 right column).

Regarding claim 53, it is noted that this claim recites similar features called for in claim 25 lines 5-8. Thus, claim 53 is also rejected for the same reason as set forth in claim 25 above.

Regarding claim 54, Masaki further teaches even positions within the row (see figure 6a: even positions "26" (coordinated at x=2, y=2 with regard to the origin at "29" (bottom left corner of the 8x8 block)) and "28" (coordinated at x=4, y=2) within the 2nd row (row of "25, 26, 27, 28, 28, 27, 26,25")) and odd position within the row (see figure 6a: odd positions of "21" (Likewise, coordinated at x=1, y=3) and "23" (Likewise, coordinated at x=3, y=3) within a 3rd row (row of "21, 22, 23, 24, 24, 23, 22, 21")).

Regarding claim 55, Masaki further teaches the pixel values each comprises a respective encoded pixel value (see figure 6 and text portion mentioned under "Transposition Memory" section on page 391 right column. Note the pixel values stored in the transposition memory (transposed data) refer to encoded pixel values order for the IDCT to inverses its original value).

Regarding claim 56, Masaki further teaches DCT coefficient (this features is inherently included in the "encoding/decoding" mentioned on page 387, right column, lines 1-3).

Regarding claim 57, Masaki further teaches extracting the row of pixel values from a zigzag-encoded block of pixel values (see figure 6: Note the data block shown in figure 6 refers

to the so called "zigzag-encoded block of pixels and these data block are extracted according to the text portion mentioned under "Transposition Memory" section on page 391 right column).

Regarding claims 58-59, Masaki further teaches inverse discrete cosine transform values (see 1-D IDCT shown in figure 7).

6. Claims 5-7 and 34-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 15-24 and 43-52 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 5, the closest prior art (Masaki) does not teach the features recited in lines 7-10. Claim 34 is allowable for the same reasons as claim 5.

Regarding claim 6, the closest prior art (Masaki) does not teach the features recited in lines 7-12. Claim 35 is allowable for the same reasons as claim 6.

Regarding claim 7, the closest prior art (Masaki) does not teach the features recited in lines 8-15. Claim 36 is allowable for the same reasons as claim 7.

Regarding claim 15, the closest prior art (Masaki) does not teach the features recited in lines 4-12. Depend claims 16-24 are allowed for the same reasons as claim 15.

Regarding claim 43, the closest prior art (Masaki) does not teach the features recited in lines 2-12. Dependent claims 44-52 allowed for the same reasons as claim 43.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duy M. Dang whose telephone number is 571-272-7389. The examiner can normally be reached on Monday to Friday from 5:30AM to 2:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso can be reached on 571-272-7695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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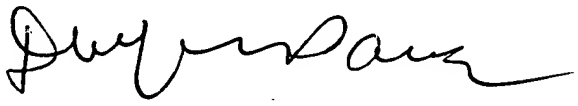

Duy M. Dang
Patent Examiner